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Dimmable CFL using the UBA2027X family

Rev. 1 — 15 August 2011

Application note

NXP

Revision history

Rev	Date	Description
v.1	20110815	first issue

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1. Introduction

This application note describes the design of a dimmable CFL with a low dimming level using the UBA20270 or UBA20271/UBA20272 ICs. The example illustrated is a 20 W application using the UBA20270 with SPS04N60C3 external MOSFETs. At power levels below 20 W, the UBA20271/2 with integrated MOSFETs can be used.

The UBA20270 controller can be used with both the 120 V and 230 V mains voltage applications. Select the UBA20272 for 230 V mains applications and the UBA20271 for 120 V mains applications for optimal performance.

Remark: Unless otherwise stated all voltages are AC.

A standard commercially available phase-cut wall dimmer is used as the triac wall dimmer. This type of dimmer is representative of most dimmers for 120 V or 230 V input mains applications. Some component values in the application need adapting for dimming compatibility when using other dimmers.

The topology is based on a Voltage Source Charge Pump (VSCP) that is intended to create the necessary hold current for the triac in the dimmer. An End of Life (EOL) circuit has been added externally to the main board for evaluation. The circuit senses high lamp voltage and can shut down the IC in the burn state. No ignition or high ignition voltage is monitored by the coil saturation protection in the IC.

2. Scope

This application note is organized as follows:

- Section 3 describes the basic operation of triac dimming
- Section 4 describes application design
- Section 5 Appendix 1: power calculation equations
- Section 6 Appendix 3: inductive mode preheat calculations

3. Triac dimming

3.1 Triac dimmer circuit

Figure 1 shows the circuit diagram of a triac wall dimmer used in 120 V (RMS) applications.

Fig 1.   Triac wall dimmer with LC filter
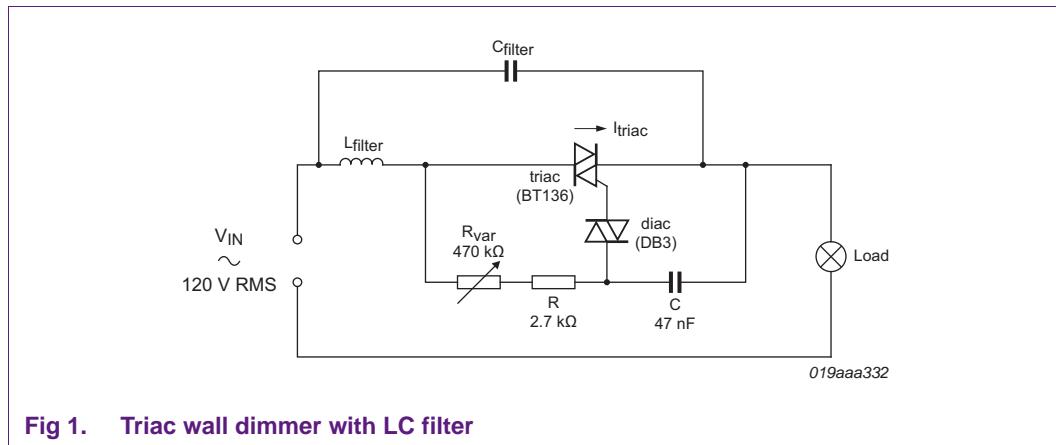
The triac shown in Figure 1 employs forward phase-cut dimming. CFL loads such as incandescent lamps are only energized during the last part of each power-line half cycle (α to π and $\alpha + \pi$ to $2\,\pi$). See Figure 2 for details.


Fig 2.   Triac with phase-cut dimming angle α
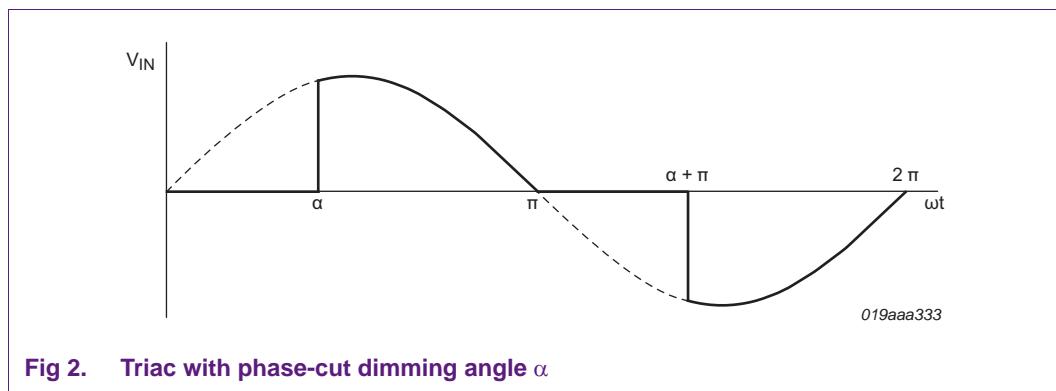
3.1.1 Circuit overview

In Figure 1, the capacitor C (47 nF) is charged using a fixed resistor R (2.7 kΩ) and a variable resistor R_{var} (470 kΩ). R_{var} (470 kΩ) sets the phase-cut dimming angle.

When the resistance is low, the capacitor charges quickly. As the voltage across the capacitor reaches the diac break-over voltage, the triac fires and the current I_{triac} flows. The current in the load must be as high as the triac latching current within the period the gate of the triac is fired or triggered. This current continues to flow until I_{triac} drops below its minimum hold current I_H.

If the triac latching current is not reached by the end of its gate trigger pulse, multiple triac firing can occur in a mains half cycle. Avoid multiple firings because they generate unwanted audible noise while the lamp is dimmed.

When the load is an incandescent lamp (resistive load), there is no phase shift between lamp voltage and lamp current. The current can rise high enough within the trigger period of the triac. However, for CFLs, it is not true because of the capacitor in the input filter and the buffer capacitor. The triac is a bidirectional device which operates in two quadrants (see Figure 3). During the negative half cycle, the same process as described earlier is repeated.
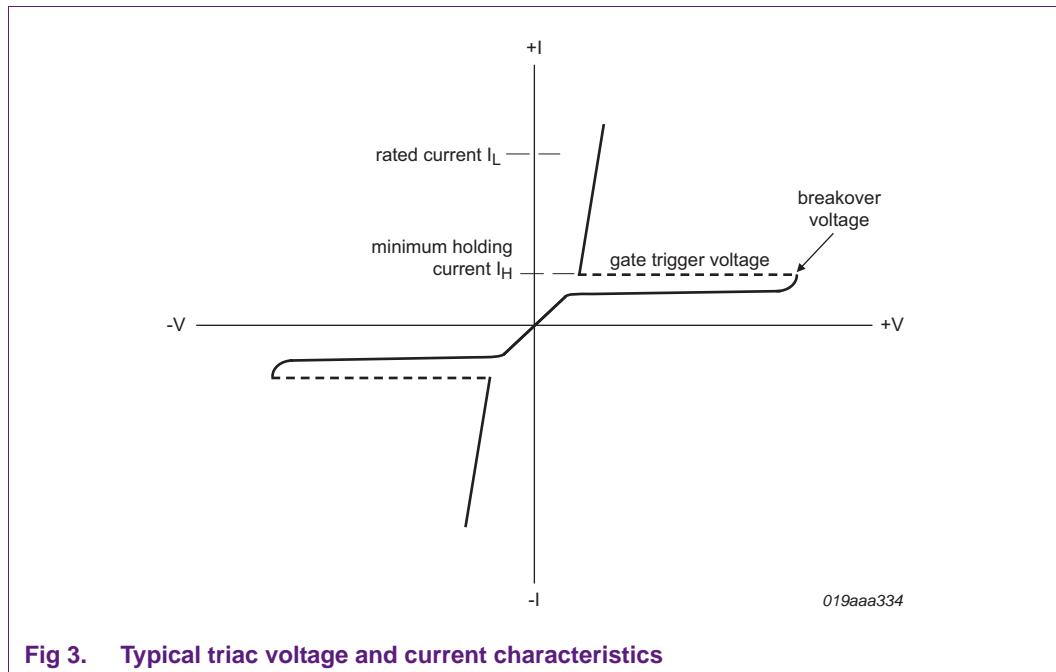
Fig 3. **Typical triac voltage and current characteristics**

In the triac application, the L_{filter} and C_{filter} can produce ringing of the triac current when the triac latches after a step response. The L_{filter} and C_{filter} is the LC filter in CFL applications. The triac ringing current must remain above I_H ensuring the triac remains powered up.

3.2 Triac wall dimmer with VSCP and CFL ballast

Figure 4 shows a triac wall dimmer with VSCP and CFL ballast. The half-bridge MOSFETs in the circuit switch the resonant tank circuit while the lamp voltage generates the triac boost or hold current. The relevant waveforms are shown in Section 6 on page 31 (see Figure 25).

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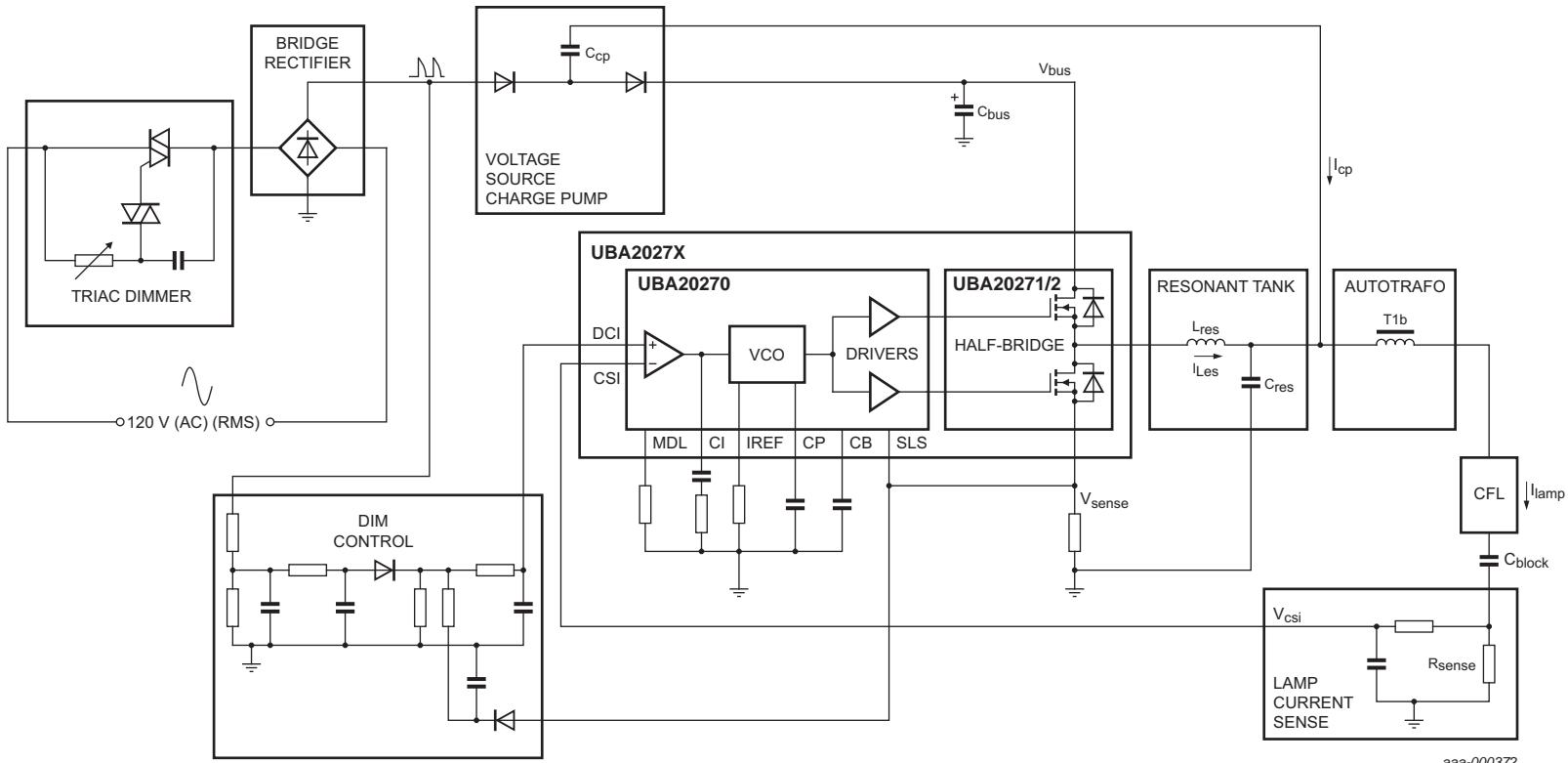
Fig 4.   Triac wall dimmer with VSCP and CFL ballast

The VSCP maintains triac conduction even at deep dimming since I_H is exceeded for low phase-cut angles (down to. A = 130°). A minimum hold current of 30 mA to 50 mA is sufficient for most triac dimmers. With a triac phase angle (A), the input voltage, boost and average boost current is shown in Figure 5.

(1) V_{IN}
(2) I_{bst}
(3) $I_{bst(av)}$

Fig 5.   Input waveforms as function of phase cut angle α
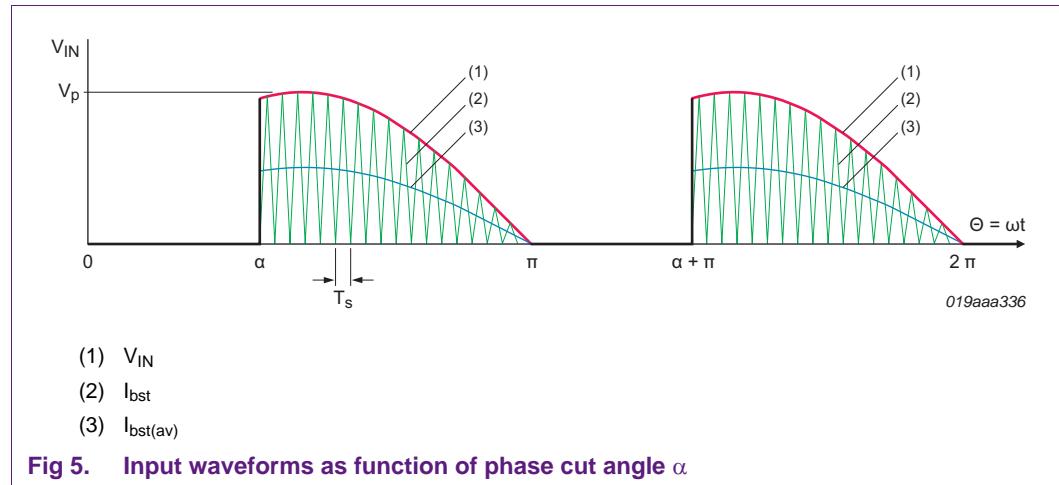
The VSCP operates in discontinuous mode and the average input boost current follows the input mains voltage.

The dimming control signal for the DCI pin is derived from the average of the mains rectified signal. This control signal decreases during dimming and simultaneously the frequency regulation loop of the IC increases the frequency of the half-bridge. These actions ensure the voltage on the CSI and DCI pins are equal at 0.34 V as shown in Section 4.6.

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4. Application design

4.1 Block diagram

[Figure 6](#) shows the basic block diagram of the UBA20270 controller in a 230 V application including VSCP and hold current pump. The triac hold current pump increase triac hold current and therefore dimming stability.
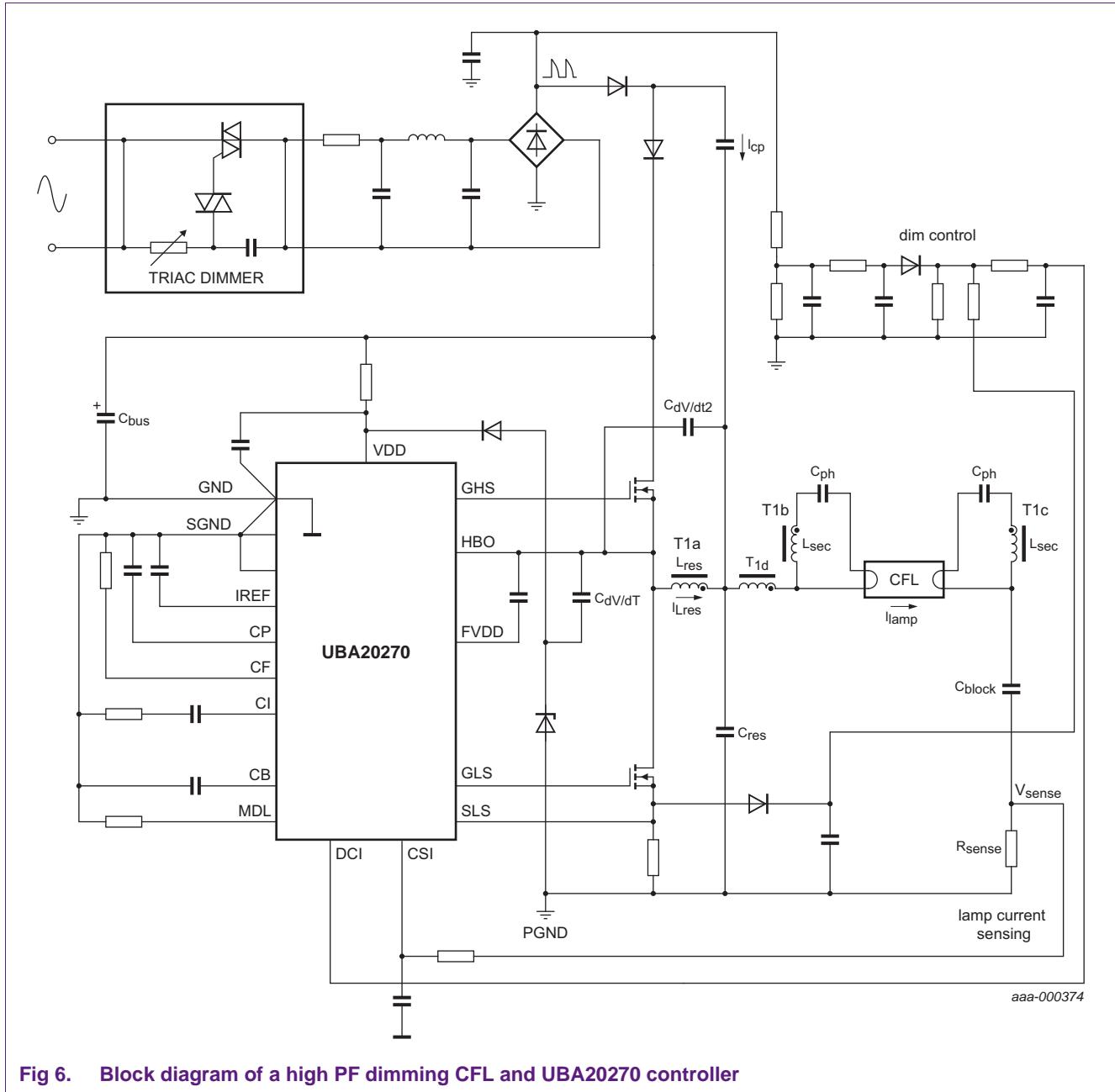
Fig 6. **Block diagram of a high PF dimming CFL and UBA20270 controller**

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4.2 Resonant tank parameters

The resonant inductor (L_{res}) is the dominating component for the power delivered to the lamp (P_{lamp}), however, the resonant capacitor (C_{res}) also has influence. Calculate the L_{res} value to deliver the required lamp current during the boost period. The lamp current during boost is 1.5 times the nominal lamp current. C_{res} is calculated to ensure that the operating frequency is above 40 kHz in the boost state and the minimum mains voltage is V_{mains} −10 %.

The current in the MOSFETs increases for larger a C_{res}. At a smaller C_{res}, the possibility of hard switching increases because the resonant tank is no longer inductive.

The autotransformer concept lowers the MOSFET current by reducing the voltage on C_{res} while maintaining the nominal lamp voltage.

An important parameter is the parasitic capacitance inside the transformer L_{res} and its secondary windings. Parasitic capacitance is especially important for the filament winding connected to the lamp current sense resistor R_{CSI}. Due to parasitic capacitance, current is directly injected from the resonant tank into R_{CSI}, bypassing the lamp discharge current.

This current degrades deep dimming performance because the lamp discharge current is no longer regulated. To ensure good deep dimming performance, the parasitic capacitance must be less than 25 pF.

When the autotransformer winding is used in series with R_{CSI}, the capacitance between L_{res} and winding T1d must be less than 25 pF. See Section 4.3 for more information.

Table 1 and Table 2 list the resonant tank parameter starting values for 230 V and 120 V mains.

Table 1.   Resonant tank values 230 V mains
Applicable to all values: C_{res} = 4.7 nF, C_{block} = 47 nF and C_{CP} = 3.3 nF.

P_{IN} (W)	P_{lamp} (W)	V_{lamp} (V)	I_{lamp} (mA)	L_{res} with boost (mH)	L_{res} without boost (mH)
15	13	105	120	2.5	2.7
18	16	100	160	2	2.5
20	18	110	160	2	2
23	21	110	190	2	2

Table 2.   Resonant tank values 120 V mains
Applicable to all values: C_{block} = 22 nF and C_{CP} = 3.3 nF.

P_{IN} (W)	P_{lamp} (W)	V_{lamp} (V)	I_{lamp} (mA)	L_{res} with boost (mH)	L_{res} without boost (mH)
13	11	100	110	1.2[1]	1.2
15	13	105	120	-[1]	1.2
15	13	105	120	1[2]	-
20	18	110	160	-[2][3]	1

[1] C_{res} = 5.6 nF.

[2] C_{res} = 6.8 nF.

[3]   Not recommended for resonant topology. Use voltage doubler topology instead.

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4.3 Autotransformer

An autotransformer is concept where the primary winding of a transformer is tapped somewhere on the primary winding to generate a lower secondary voltage. Since a transformer works both ways using the center tap as primary, you can also raise the voltage. The disadvantage of the autotransformer is that the primary and secondary are non-isolated. However, when use in a CFL application, this fact is not a problem.


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Fig 7.   VSCP with auto-transformer T1d
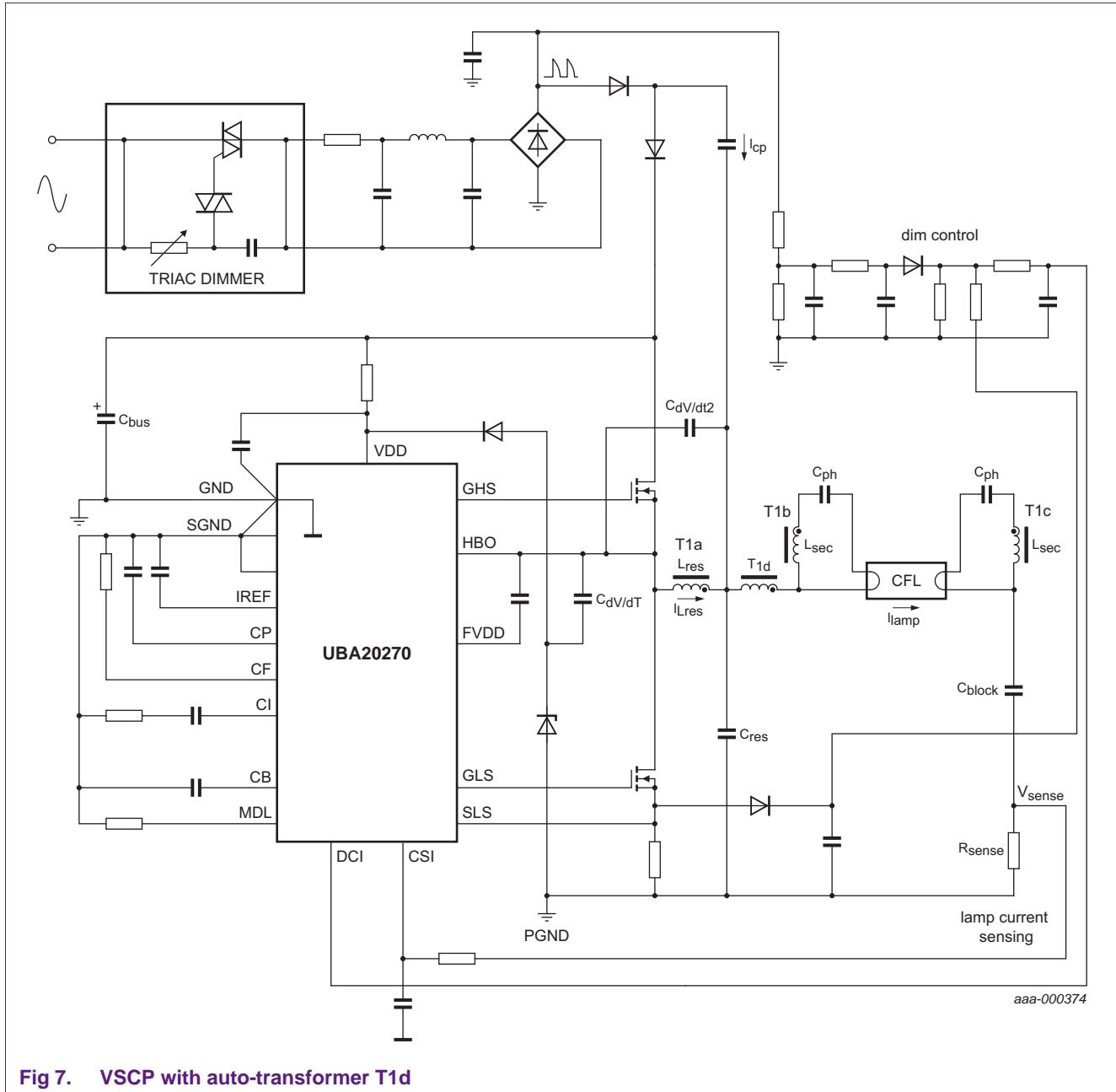
The autotransformer concept is mainly for the 120 V resonant topology. The concept reduces the reactive half-bridge loading by lowering the voltage on the resonant capacitor. In doing so, overall efficiency improves by 30 %.

When a burner with a low lamp voltage (< 95 V) is fitted, the same topology can increase the lamp voltage on the resonant capacitor. The topology ensures that the voltage source charge pump can generate the required hold current.

In all applications, the output voltage of the secondary winding of the autotransformer is set at 20 V (RMS). The nominal lamp voltage increases/reduces, depending on how the primary and secondary winding are added in series.

Remark: If the voltage is increased/reduced, note the dots in the transformer windings because they determine how the windings are used in the schematics: Figure 21, Figure 22, Figure 23 and Figure 24.

Use the autotransformer for 120 V mains in two cases and when the nominal lamp voltage is:

- \> 110 V: to lower the voltage on the resonant tank
- < 95 V: to increase the voltage on the resonant tank

Table 3.   Transformer ratios for 230 V and 120 V mains

L_{res} with boost (mH)	T1d ratio (L_{res} : T1d)	L_{res} without boost (mH)	T1d ratio (L_{res} : T1d)
Transformer ratio 230 V			
2	9.74 : 1	2.5	9.44 : 1
2.5	9.44 : 1	2.7	10.27 : 1
Transformer ratio 120 V			
1	7.26 : 1	1.2	6.84 : 1

4.4 Step dimming

For no dimming ($\alpha = 0$) the average input current delivered by the charge pump. Input current and input power are as shown in Equation 1 and Equation 2:

Input current:

$$|I_i| = C_{CP} \times f_s \times (|V_p| + 2V_{lamp} - V_{bus}) \tag{1}$$

Input power:

$$P_{IN} = \cfrac{1}{2 \times C_{CP} \times f_s \times V_p^2 + \cfrac{2}{\pi} \times C_{CP} \times f_s \times V_p \times (2V_{lamp} - V_{bus})} \tag{2}$$

Where: V_p = peak input voltage, f_s = the half-bridge switching cycle, V_{bus} = bus voltage and α = triac firing angle (see Figure 5). See Ref. 3 for further information.

The power delivered to the lamp is:

$$P_{lamp} = \frac{V_{lamp}^2}{\omega_s L_{res}} \sqrt{ \left(\frac{\sqrt{2 \cdot V_{bus}}}{\pi \cdot V_{lamp}} \right)^2 (1 - \omega_s^2 L_{res} C)^2 - (1 - \omega_s^2 L_{res}(C + C_{res}))^2 } \tag{3}$$

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Where: $\omega_s = 2\pi f_s$; V_{lamp} = lamp RMS voltage, L_{res} = resonant indicator and C_{res} = resonant capacitor. C = inductive mode heating circuit secondary capacitance which is transferred to the primary side.

The expression for P_{lamp} in Equation 3 has been derived using the equivalent circuit shown in Figure 8.
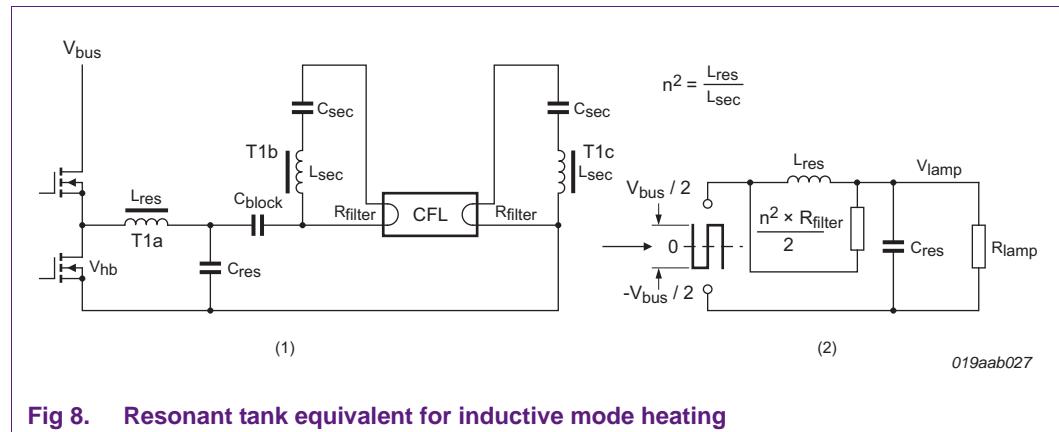

Fig 8.   Resonant tank equivalent for inductive mode heating

$$V_{hb} = \frac{\sqrt{2}}{\pi} V_{bus}(\text{RMS}) \tag{4}$$

$$R = R_{filter} \times \frac{L_{res}}{2} \times L_{sec} \tag{5}$$

$$R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}} \tag{6}$$

The power delivered from the mains by the V_{SCP} and delivered to the lamp is: $P_{lamp} = \eta \times P_{IN}$

The value of C_{res} = 4.7 nF together with L_{res}:

$$R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}} \tag{7}$$

and $C_{dV/dt}$ is chosen so that the resonant tank remains inductive over the complete dimming range, that is, high-bridge current lags the half-bridge voltage. For a nominal lamp power of 21 W, the phase lags half-bridge voltage is 51°, calculations are shown in Section 6.

The instantaneous current in each MOSFET which is $I_{CP} - I_{hb}$ is calculated in Section 6.

The RMS current is approximately 410 mA which agrees with measurements. The instantaneous current $I_{CP} - I_{hb}$ together with the $C_{dV/dt}$ capacitor determine the rise (t_r) and fall (t_f) time of the half-bridge voltage according to Equation 8:

$$\frac{I_{CP} - I_{hb}}{C_{dV/\text{dt}}} = \frac{V_{bus}}{t_{no(r)} \ or \ t_{no(f)}} \tag{8}$$

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Using a 470 pF capacitor, the rising/falling non-overlap time ($t_{no(r)}$ or $t_{no(f)}$) remains within specification. This is necessary to maintain Zero Voltage Switching (ZVS) that is, no hard switching.

4.5 Inductive mode preheating and SoS

Correctly preheating the filament is necessary to ensure long lamp operating life and provides the advantage a lower ignition voltage.

The preheat time is applied to the filaments during the preheat period and is set using Equation 9:

$$t_{ph} = \frac{C_{CP}}{I_{o(CP)}} \times \left(\frac{16 \times V_{hys(CP)}}{5 - V_{th(CP)max}} \right) \tag{9}$$

Where: C_{CP} = 330 nF, $I_{o(CP)}$ = 5.9 µA, $V_{hys(CP)}$ = 0.7 V, and $V_{th(CP)max}$ = 4.5 V. The preheat time is 0.67 s.

The preheat frequency can be set by measuring the voltage across the SLS resistor between the source and ground of the lower MOSFET. See Figure 24. The half-bridge frequency starts at $f_{VCO(max)}$ and sweeps down until the voltage on the SLS pin reaches the V_{ph} level that is defined in the specification. The sweep then stops for the duration of the preheat time t_{ph}.

During the preheat time, the frequency is controlled so that the voltage on the SLS pin stays constant, implying that the half-bridge current is kept constant. The half-bridge current level can be adapted by changing the value of the SLS resistor. However, the value selected must not cause the lamp to ignite during the preheat time. Also the saturation protection and overcurrent protection use the same resistor. Therefore, practical values for R_{SLS} for 120 V mains are between 0.9 Ω and 1.5. Values for 230 V mains are between 1.5 Ω and 2.2 Ω. Too low a value and the lamp voltage is too high during low mains. Too high a value and saturation protection is triggered.

If the preheat energy or SoS are not within limits, the secondary turns or the secondary capacitors need to be adjusted.

The frequency versus time is shown in Figure 9.

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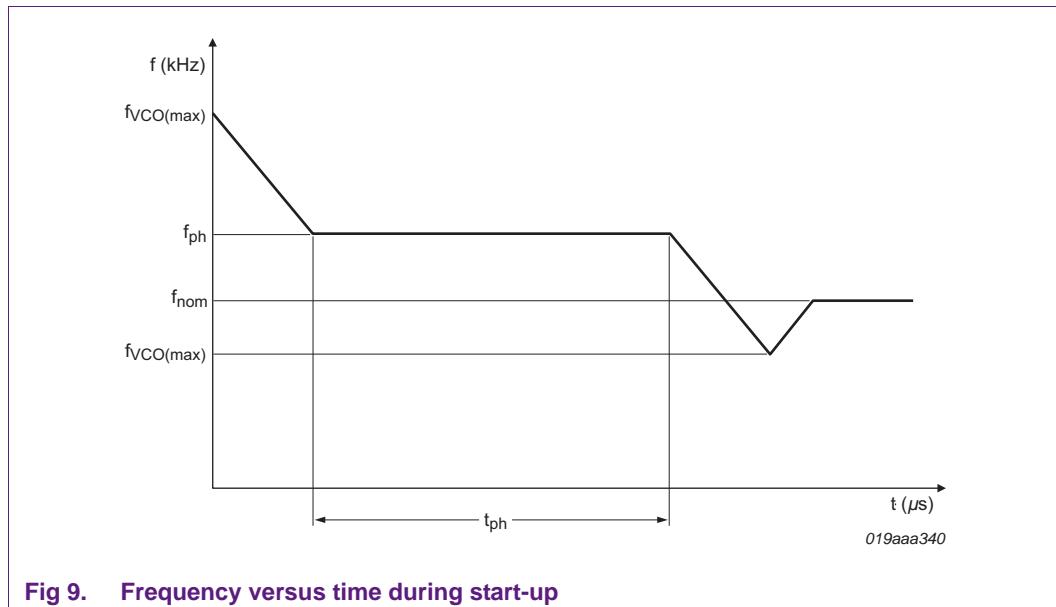
Fig 9. **Frequency versus time during start-up**

For inductive mode heating, the relationship for the preheat (filament) current is calculated in Section 6.

For example, when the half-bridge frequency is 71 kHz, non-overlap time is 1.5 μs and the RMS filament current is 0.25 A. Then the filament power dissipated is approximately 1.6 W when the hot filament resistance $R_{filter} = 25\ \Omega$. The power supplied to the filament during preheat is $f_sCV^2_{sec}$ and for a capacitance of 47 nF:

$$V_{sec} = \frac{V_{pri}}{n} \tag{10}$$

where V_{pri} = 350 V and:

$$n = \sqrt{\frac{L_{res}}{L_{sec}}} = 16 \tag{11}$$

Then power supplied to filament is approximately 1.6 W.

To guarantee sufficient filament current is provided at the end of the preheat period, the hot to cold ratio of filament resistance must be preferably 4.75 : 1. If however, this conflicts with the SoS at deep dimming, choose a lower value of 4 : 1. A higher value can overload the filament and reduce the operating life time. After the preheat period, the frequency falls and the lamp ignites when the ignition frequency f_{ign} is reached. The lamp can be modeled now as a (negative) resistance where:

$$R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}} \tag{12}$$

Before ignition, the lamp has a much higher impedance as no lamp current is flowing. Both characteristics are shown in Figure 10.

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Capacitor C_{CF}, resistor R_{IREF} and the voltage at the CI pin determine the internal Voltage Controlled Oscillator (VCO) frequency (half-bridge frequency). The minimum and maximum frequencies are as defined in Equation 13:

$$f_{VCO(min)} = 40.5 \times 10^3 \cdot \left(\frac{100 \times 10^{-12}}{C_{CF}} \right) \cdot \left(\frac{33 \times 10^3}{R_{IREF}} \right) and \, f_{VCO(max)} = 2.5 \times f_{min} \qquad (13)$$

Where: P_{lamp} = 20 W, V_{lamp} = 110 V; L_{res} = 2·10^{-3}, L_{sec} = 10·10^{-6} and C_{res} = 4.7·10^{-9}

$$R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}} \qquad (14)$$

Where: R_{lamp} = 605 and C_{sec} = 33·10^{-9}

$$C_p = 2 \cdot C_{sec} \cdot \frac{L_{sec}}{L_{res}} \qquad (15)$$

Where: C_p = 2.4 × 10^{-10}, f = 00000, 00200 to 80000 and $\omega(f)$ = 2·π·f and p(ω) = j · ω.

(1) H(2·π·f 2000).
(2) H(2·π·f 605).

Fig 10. Transfer of frequency before and after ignition
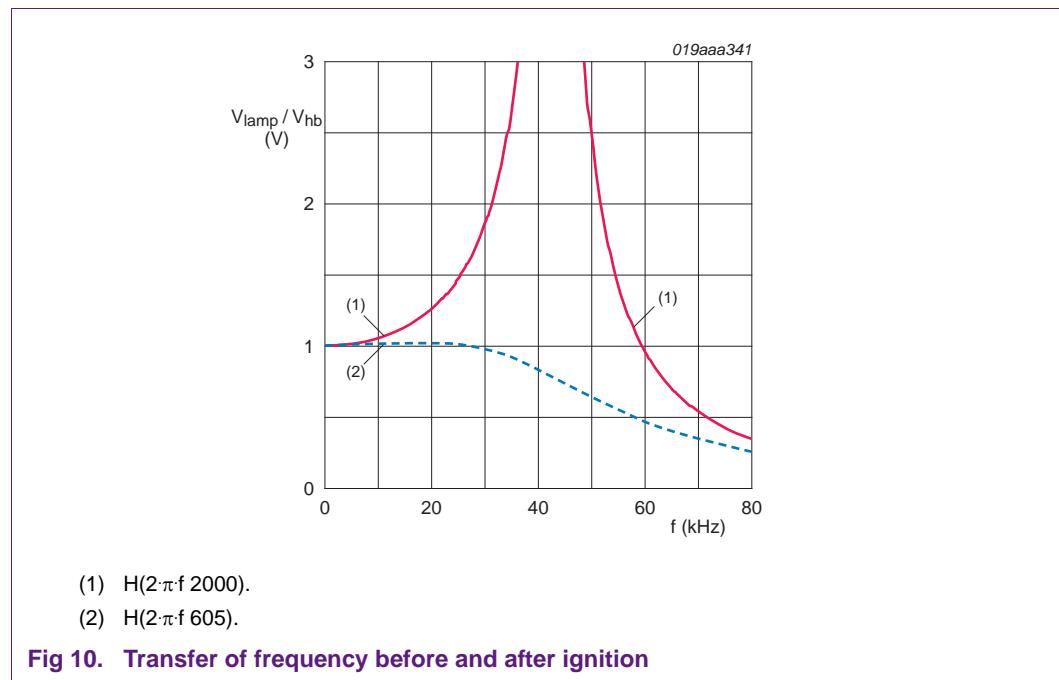
After lamp ignition, the filaments must have enough supplied power in order to maintain an optimum temperature over the complete dimming range. Too low a temperature and sputtering or local hot spots occur resulting in damage to the filament. Too high a temperature causes evaporation of the filament over a longer period. The Sum of Squares (SoS) is a measure of the expected amount of heat generated in the filaments and is expressed as SoS = I^2_{LL} + I^2_{LH}. Figure 11 shows the waveform direction of I_{LL} and I_{LH} against time for period the filaments are inductively preheated.

SoS must remain between the minimum and maximum setting as specified by the lamp manufacturer. However, a SoS setting close to the target setting is preferred for optimal long life operation of the lamp. Maintain within specification adequate filament preheating and optimum SoS but in practice, they are conflicting requirements. Further information can be found in Ref. 2.
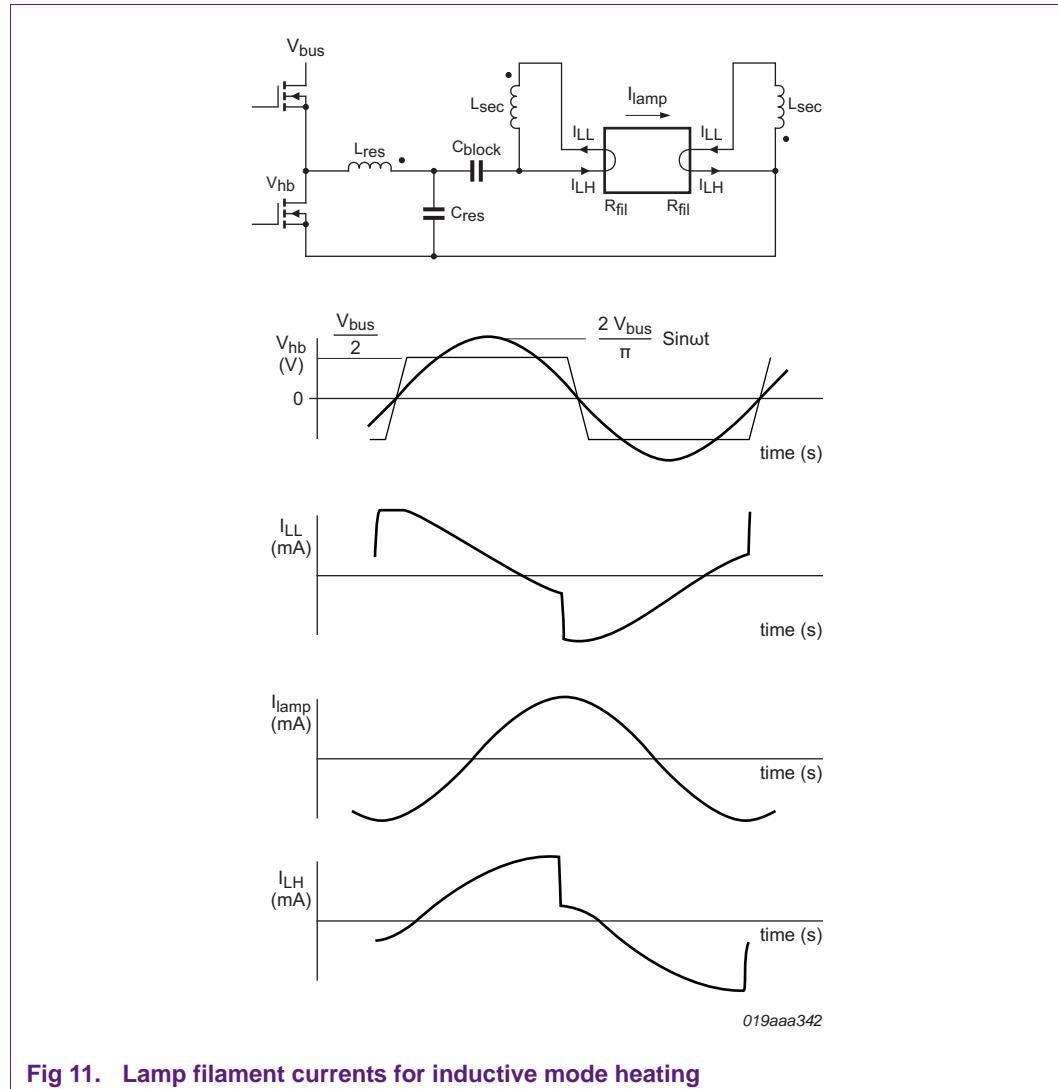

Fig 11.   Lamp filament currents for inductive mode heating

4.6 Dimming using frequency feedback control loop

After lamp ignition and when the IC is in the burn state, the internal average current sensor at the CSI pin is compared with the DCI voltage minus an offset. The CSI pin voltage is derived by sensing the lamp current and converting it to voltage using a sense resistor as shown in Figure 12. This voltage is supplied to the CSI pin as $V_{i(CSI)} = I_{lamp(RMS)} \cdot R_{SENSE}$. The high frequency feed through in the transformer and ignition spike is reduced by adding low pass filter. After R_{SENSE}, the −3 dB point of the filter is set to 1.5 MHz.

The maximum voltage on the CSI pin is clamped at 1 V (RMS). This means that the nominal lamp current is calculated using $I_{lamp(RMS)} = 1/R_{SENSE}$.
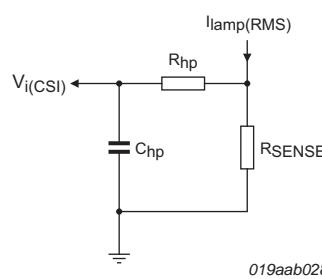
Fig 12. Lamp current sensing

The DCI pin voltage is derived from the mains rectified signal as shown in Figure 13. This feature gives a dimming voltage range of 0.24 V to 1.5 V for a phase-cut range of α = 0° − 15° to 120°. This voltage (after being averaged with the double filter C8, C10, R5 and R6) is applied to the DCI pin where:

Table 4. Component values

Component	230 V	120 V
R8	220 kΩ	120 kΩ
R9	220 kΩ	100 kΩ
R10	15 kΩ	15 kΩ
R11	39 kΩ	39 kΩ

The voltage on the DCI pin is set 10 % higher than the maximum of 1.34 V. This offset compensates for small line voltage variations and tolerances in the system. This compensation ensures the lamp does not dim immediately but remains at a constant output. In this set-up, the maximum lamp voltage occurs in the first 0° to 20° of the phase angle. The diac or gate trigger circuits phase-cut dimmers cannot start from 0° which always presents a small phase cut. The exact DCI can be calculated using:

$$\left(\frac{V_p R10(R5+R11) + R10(R8+R9)V_d}{R10(R5+R11) + R10(R8+R9)(R8+R9)(R5+R11)} - V_d \right) \frac{R11}{R5+R11} = V_{i(DCI)calc} \qquad (16)$$

Where Vp = the rectified peak voltage and Vd = the diode junction voltage drop.

$$V_{i(DCI)offset} = \frac{R}{R+R11}(V_{i(SLS)} - V_d) \qquad (17)$$

$$V_{i(DCI)} = V_{i(DCI)offset} + V_{i(DCI)calc} \qquad (18)$$
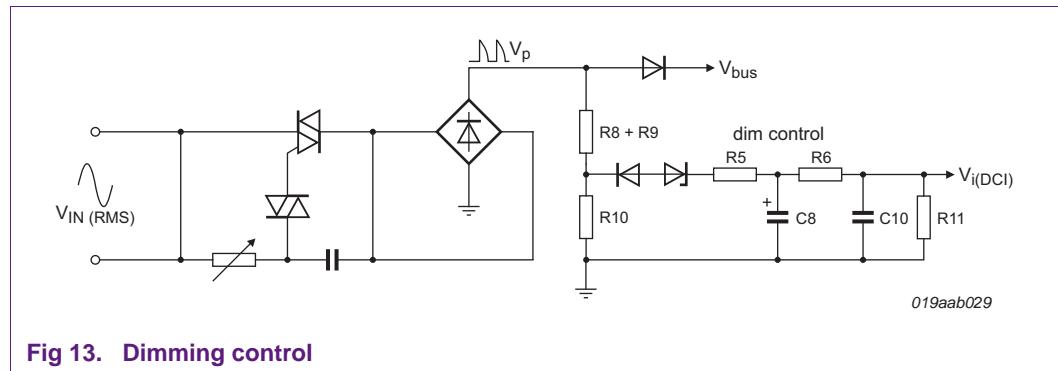
Fig 13. Dimming control

The loop regulation is in balanced when the average voltage of $V_{i(CSI)}$ is equal to $V_{i(DCI)}$ −0.34 V

During dimming, regulation is achieved with frequency control:

- $V_{i(DCI)}$ decreases
- voltage at the CI pin decreases
- frequency of the half-bridge increases
- lamp current decreases
- the average value of $V_{i(CSI)}$ decreases

Therefore the loop regulation forces the average voltage of $V_{i(CSI)}$ to follow $V_{i(DCI)}$ until an equilibrium has been reached.

4.7 Differential feedback

When using high temperature amalgam lamps flicker can be observed when the lamp is new, is cold or has been switched off for a long time. Once the lamp is warm or aged the flickering reduces and eventually disappears.

To remove this first run-up lamp flicker to a minimum differential feedback is introduced see Figure 14.

The differential feedback circuit consists of a envelope detector and the differential gain stage. The envelope detector supply comes from a secondary dV/dt supply set-up by D2b and C37 to avoid overloading the start-up resistors.

The negative envelope of the lamp current is sensed on the lamp current sense resistor R14 and low pass filtered by R38 and C29 to approximately 4 kHz. R36, R28 and C6 set the amount of differential feedback.

The circuit in Figure 14 is for a 120 V lamp, for a 230 V lamp R36 = 1.8 kΩ, R38 = 2.2 kΩ and C6 = 220 nF. Special tools are available to tailor this circuit to the lamp parameters.

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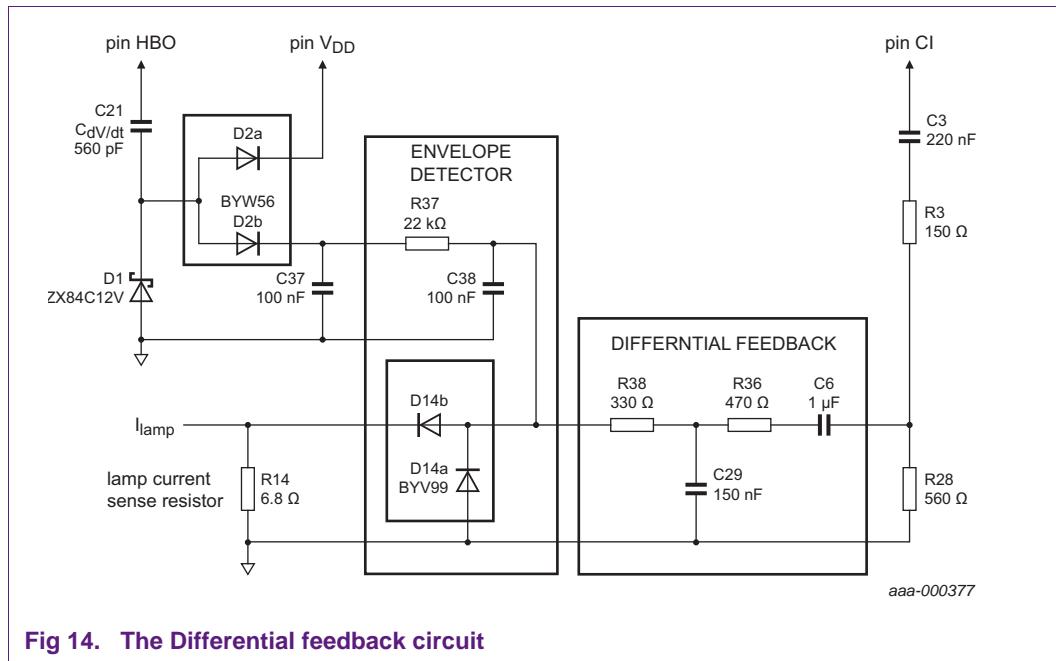
Fig 14. The Differential feedback circuit

4.8 Boosting of the lamp

When first switched on (in the first 180 s), Amalgam lamps have a slow run up or less light output. The lamp current is boosted by a fixed ratio of 1.5 : 1 to overcome this problem. The capacitor on the CB pin (C_{CB}) sets the boost time and is calculated using Equation 19.

$$t_{bst} = \frac{C_{CB}}{I_{o(CB)}} \times (126 \times V_{hys(CB)} + V_{th(CB)min} - 0.6)$$

(19)

Where: $I_{o(CB)}$ = 1 μA, $V_{hys(CB)}$ = 2.5 V, $V_{th(CB)min}$ = 1.1 V and C_{CB} = 150 nF.

These parameters lead to a boost time of 48 s. Shorting pin CB to ground turns off the boost circuit.

It is important that during the boost the filament current are still operating within their SoS limits, to avoid degrading the lamp operating life. If the lamp does not have higher current rated filaments (not intended for boost), then:

- Lower the lamp operating current to 80 % of nominal
- Run boost at 1.25 % of nominal

In simple terms, run a 12 W burner at 10 W nominal and 15 W during boost.

With higher rated lamps, set the power use the full 150 %. For example, use an 18 W burner for a 12 W lamp because the filaments automatically have a higher rating.

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4.9 Setting Minimum Dimming Level (MDL)

The minimum dim level can be used to prevent the lamp from changing over into glow phase at the lowest setting of the dimmer. Glow is observed when there is some light coming from the lamp but the CFL tube is not fully lit. This effect also causes flicker when the lamp is changing from glow to normal burn constantly. The MDL voltage is set by R_{MDL} as follows $V_{MDL} = R_{MDL} \times I_{MDL(src)}$ and is lamp-dependent.

4.10 IC Supply and capacitive mode protection

The IC starts when its supply voltage V_{DD} exceeds $V_{DD(start)}$. The first charge of the supply decoupling capacitor C_{VDD} is completed by $R_{start-up}$. This resistor must be large enough to supply at least 0.22 mA at 12.5 V. The half-bridge begins to switch and the IC is then supplied via capacitor that is connected at the half-bridge as shown in Figure 15.

A larger capacitor is required when more current is required in the external MOSFETs and thus in the internal drivers which drive the external MOSFETs. However if $C_{dV/dt}$ is too large, hard switching at higher frequencies can occur since the non-overlap time decreases at higher frequencies (adaptive non-overlap time). The minimum required value can be calculated using:

$$C_{dV/dt} = \frac{\left(2 \times the\ gate\ charge\ of\ the\ MOSFETs + \dfrac{I_{DD}}{f_{bridge(min)}} \right)}{V_{bus(min)}} \qquad (20)$$

A capacitor value of 470 pF is a good compromise between these two situations. The voltage is clamped by a 12 V Zener diode and supplied to V_{DD} via a fast recovery diode.


Fig 15. IC supply circuit

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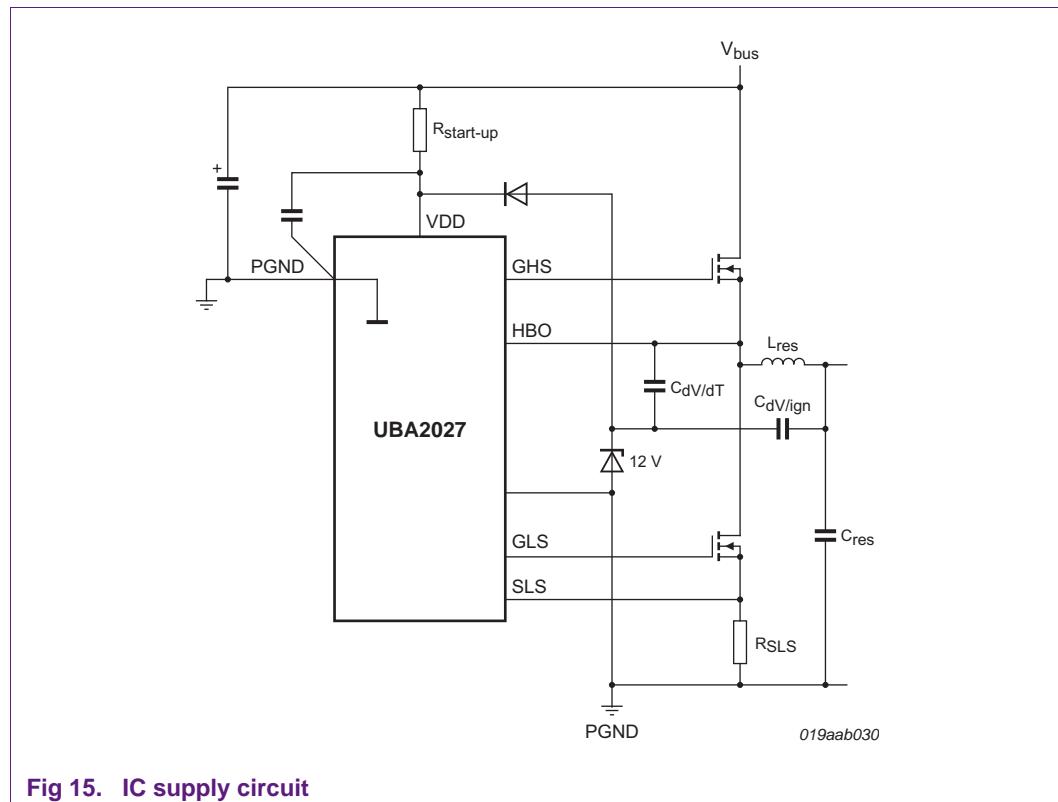
4.10.1 Capacitive mode protection

The UBA2027X checks capacitive mode operation by measuring the voltage on the SLS pin. Typical waveforms are shown in Figure 16. If after the preheat state, the voltage across R_{SLS} is higher than -5 mV when the LS MOSFET is switched on, the CMD circuit assumes capacitive mode operation at the half-bridge. To counter this operation, the half-bridge frequency is increased to $f_{VCO(max)}$.


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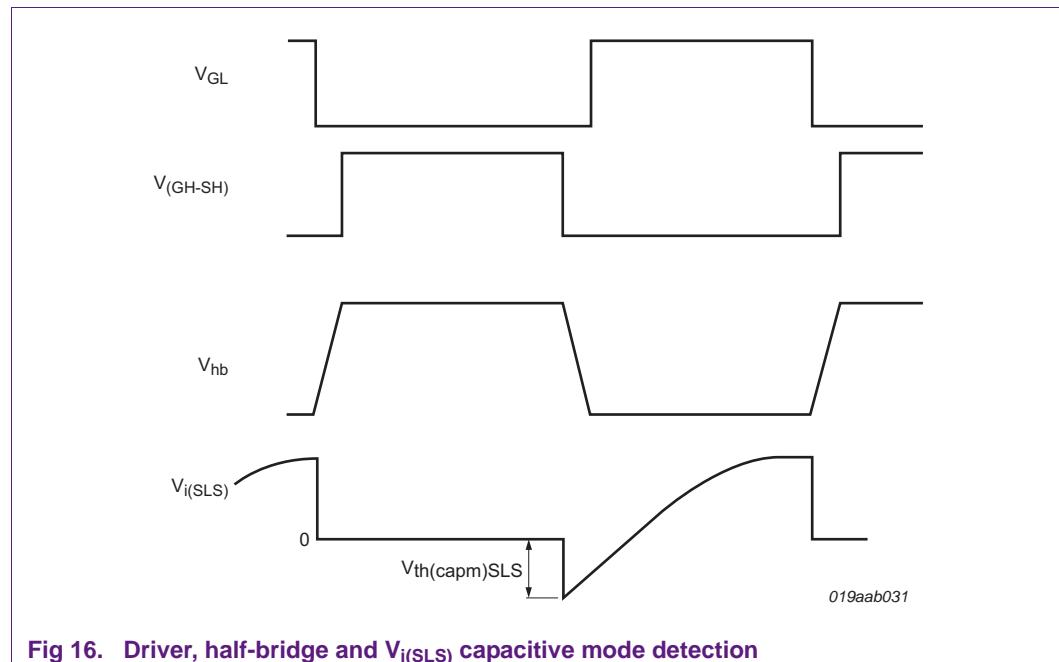
Fig 16. Driver, half-bridge and $V_{i(SLS)}$ capacitive mode detection

4.11 Mains input filtering

A Resistance, Inductance, Capacitance (RLC) filter is used to filter the mains to maintain high EMI performance at the half-bridge frequency and across the harmonic range. The inductor blocks the HF charge pump and operating current, the capacitor provides a low ohmic path for this current. HF current damping can be determined using Equation 21.

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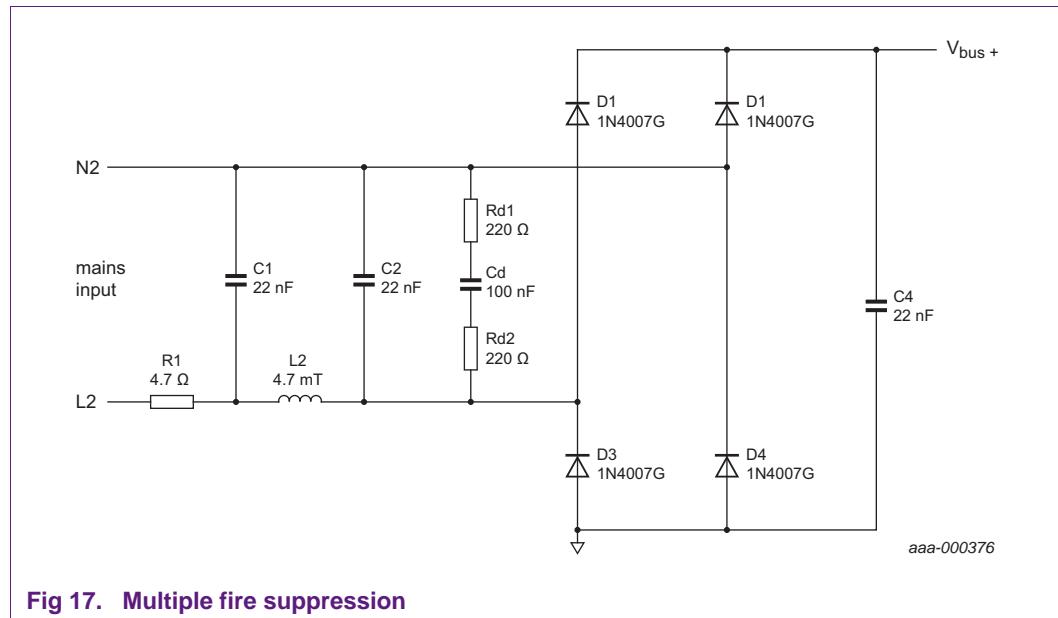
Fig 17. Multiple fire suppression

As the RLC filter does not have a constant load, the filter can also cause mains current ringing when connected to a leading-edge triac dimmer. This ringing in turn causes the triac to shut down after it is triggered once or more times causing multiple firing of the triac. The multiple firing causes unwanted audible noise. A solution for suppressing multiple fires is shown in Figure 17.

Rd1, Rd2 and C_d to create a load for the triac dimmer at higher frequencies which effectively dampens the ringing in the mains current. R_d is split in two enabling distribution of the power into small resistors.

$$20log \frac{1}{(1 + \omega^2 LC)^2 + (\omega RC)^2} \tag{21}$$

Where: L = 4.7 mH, C = 22 nF and R = 4.7 Ω. Then damping a 45 kHz relative to 50 Hz is more than 60 dB as shown in Figure 18 [a]

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a. HF current damping

b. Graphical representation

Fig 18. Transfer function input filter
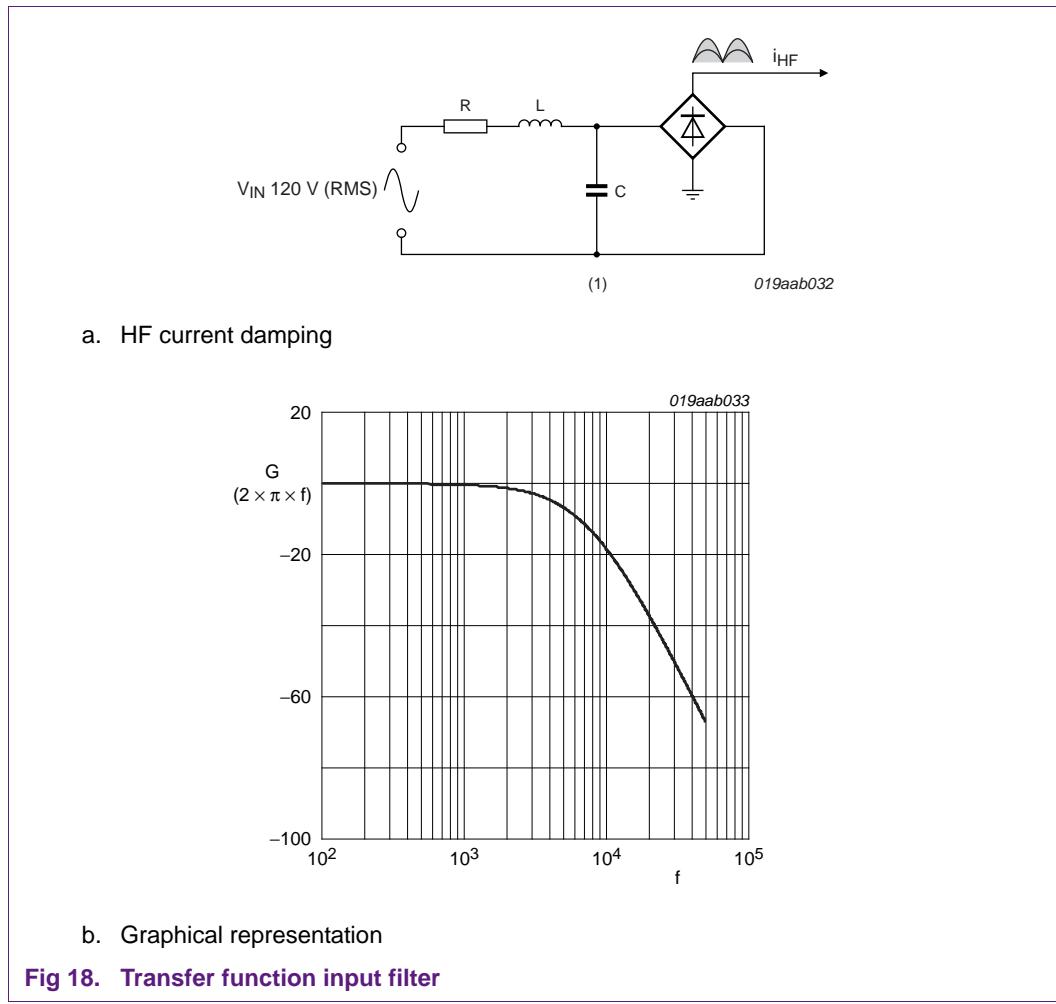
During triac operation and dimming, large transients can occur. To prevent audible noise in the circuit, a PESD15VL1BA transient suppressor is installed in parallel with inductor L.

The fused resistor R = 4.7 Ω is used to limit/damp the inrush current during start-up and during large steps of input current during triac operation. Further information can be found in Ref. 1.

4.12 Extra protections

4.12.1 OverPower Protection (OPP)

Since the measured lamp current is clamped at 1 V (RMS), the lamp current remains nominal during mains voltage fluctuations. During overvoltage conditions, the half-bridge frequency increases to maintain lamp current constant. Maintain a 10 % higher voltage level on the DCI pin than the required maximum of 1.34 V for this reason. This action resolves any AC line voltage changes in under power situations.

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4.12.2 Coil Saturation Protection (CSP) and OverCurrent Protection (OCP)

The resonant tank inductor is one of the largest components in the application therefore it is practical to select the smallest inductor possible. The maximum current capability of a coil is only important at power-up. Choose a parameter that is sufficient under CFL cold start conditions. During warm starts coil parameters are different as the core material degrades at higher temperatures. These conditions often lead to saturation of the coil when the CFL lamp is ignited. Saturation in turn leads to excessive dissipation of the half-bridge MOSFETs or even the destruction of the MOSFETs.
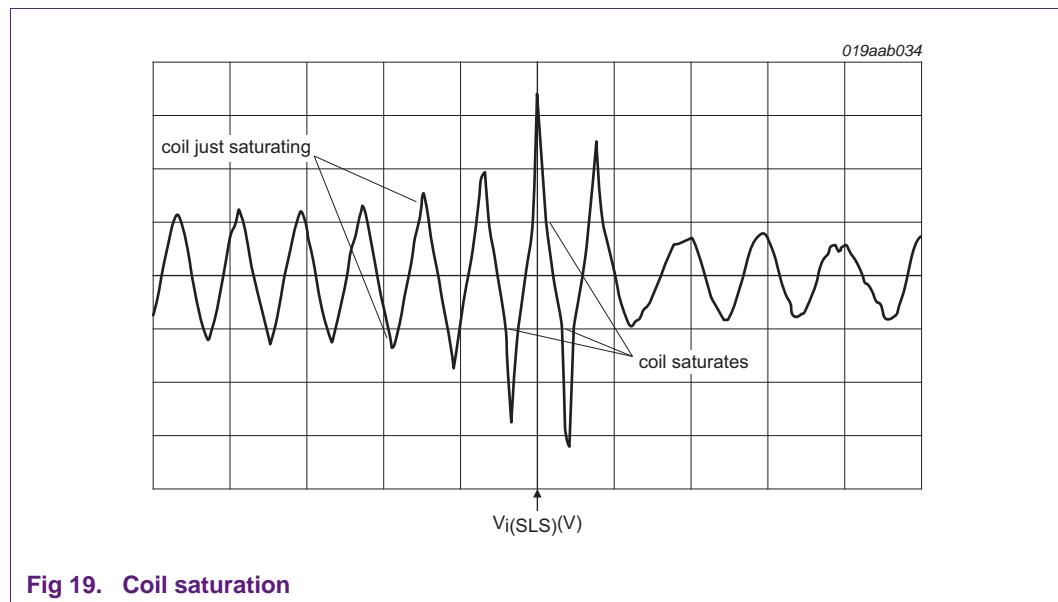
Fig 19. Coil saturation

The IC is equipped with coil saturation protection which enables the use of small inductors in the resonant tank and inverter without destroying the power MOSFETs.

The circuit monitors the current through the source of the lower MOSFET. The current forces a voltage across R_{SLS}. If the voltage is greater than a factor 2.5 V (set by R17 in Figure 22 and Figure 24) of the current during ignition, the IC limits the frequency decrease. The IC shuts down, if the lamp does not ignite within $\frac{1}{4}$ of the preheat time.

Coil saturation threshold of the IC can be adjusted to lower saturation currents.

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### 4.13 End of life circuit (optional)

The autotransformer winding can be used for an optional End Of Life (EOL) circuit when:

- T1d is not used
- when this winding is placed in series with R_{SENSE}

The EOL circuit senses a high lamp voltage during operation by sensing the voltage across the lamp inductor L_{res}. An aged (or old lamp) or a lamp which breaks during operation can cause the high voltage

The EOL circuit only works when the IC is in the burn state by pulling the CP pin below 1 V.

Adjustment of the circuit can be done by changing the value of R22
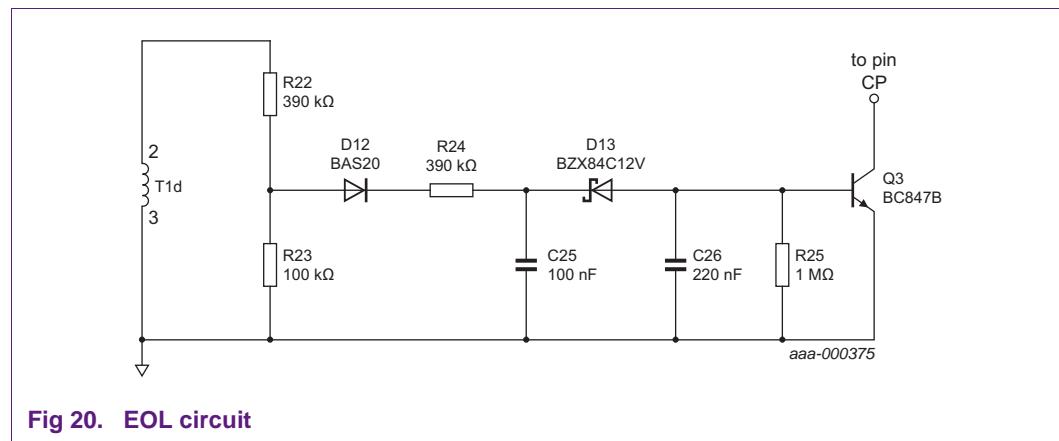
Fig 20. EOL circuit

4.14 23 W 120 V dimmable CFL schematic with UBA20270
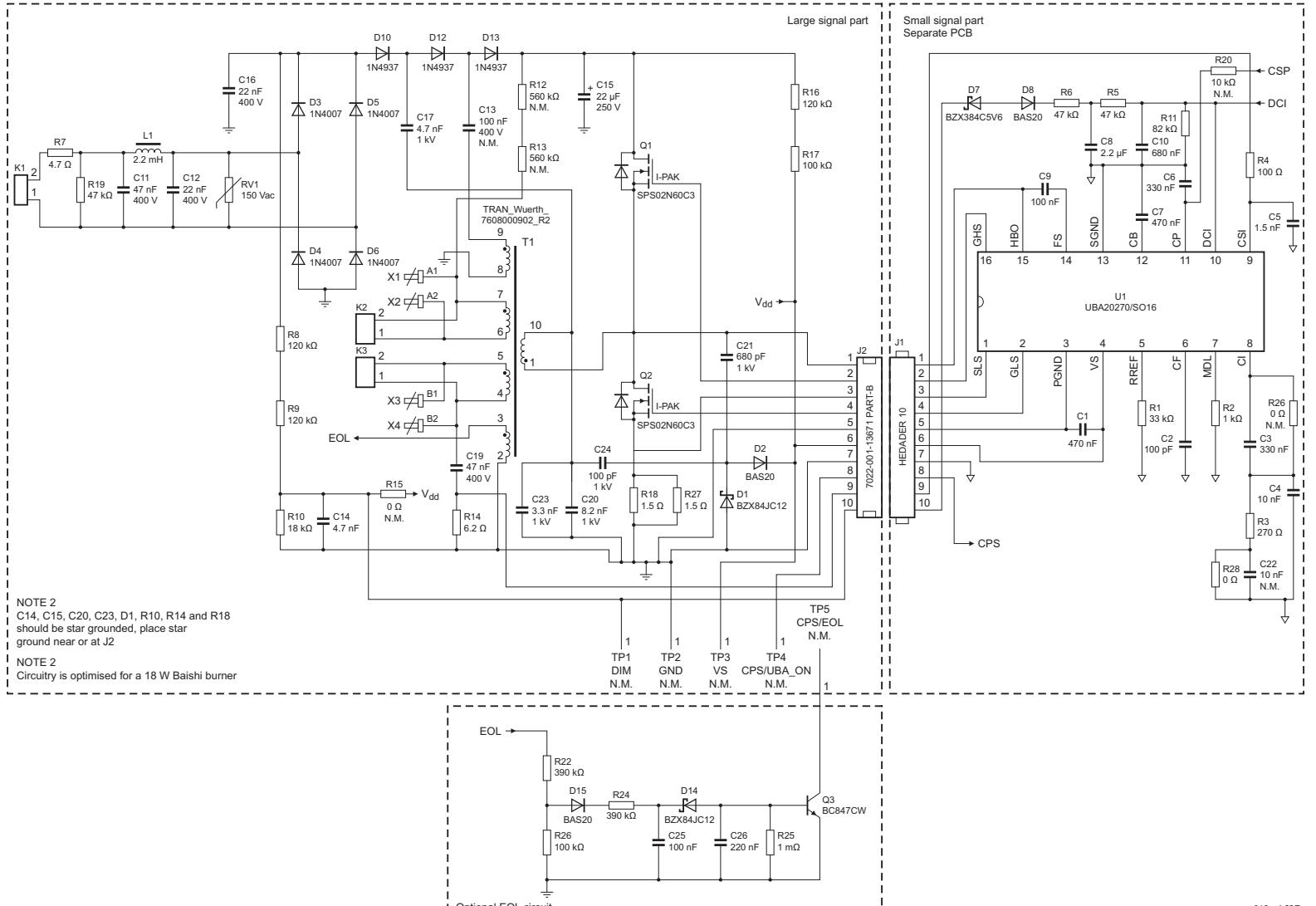
Fig 21. 23 W 120 V dimmable CFL schematic with UBA20270

Large signal part

Small signal part
Separate PCB

NOTE 2
C14, C15, C20, C23, D1, R10, R14 and R18
should be star grounded, place star
ground near or at J2

NOTE 2
Circuitry is optimised for a 18 W Baishi burner

Optional EOL circuit

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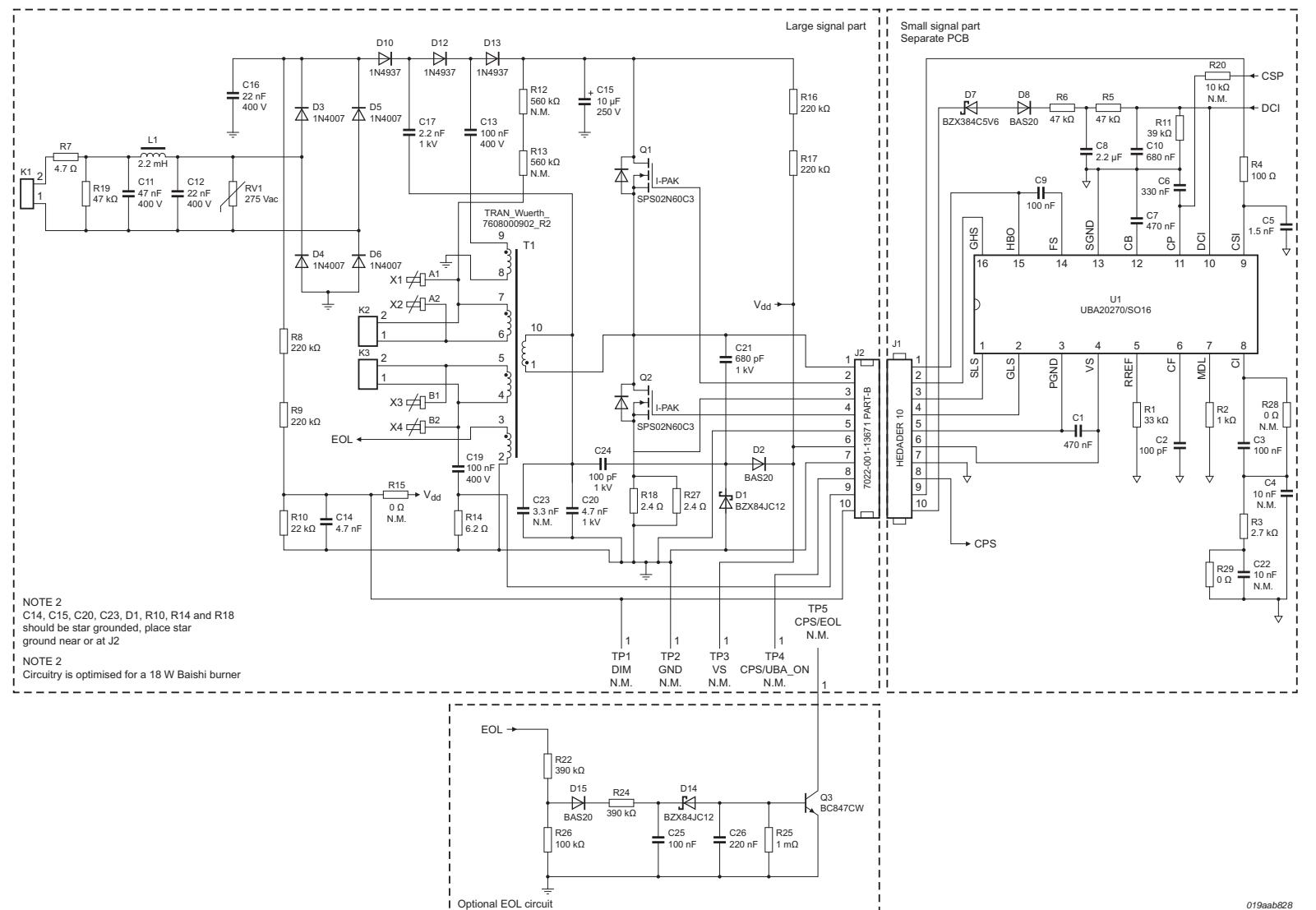
Fig 22. 23 W 230 V dimmable CFL schematic with UBA20270

4.16 18 W maximum 120 V dimmable CFL schematic with UBA20271

NOTE 2
C14, C15, C20, C23, D1, R10, R14 and R18
should be star grounded, place star
ground near or at J2

NOTE 2
Circuitry is optimised for a 18 W Biashi burner
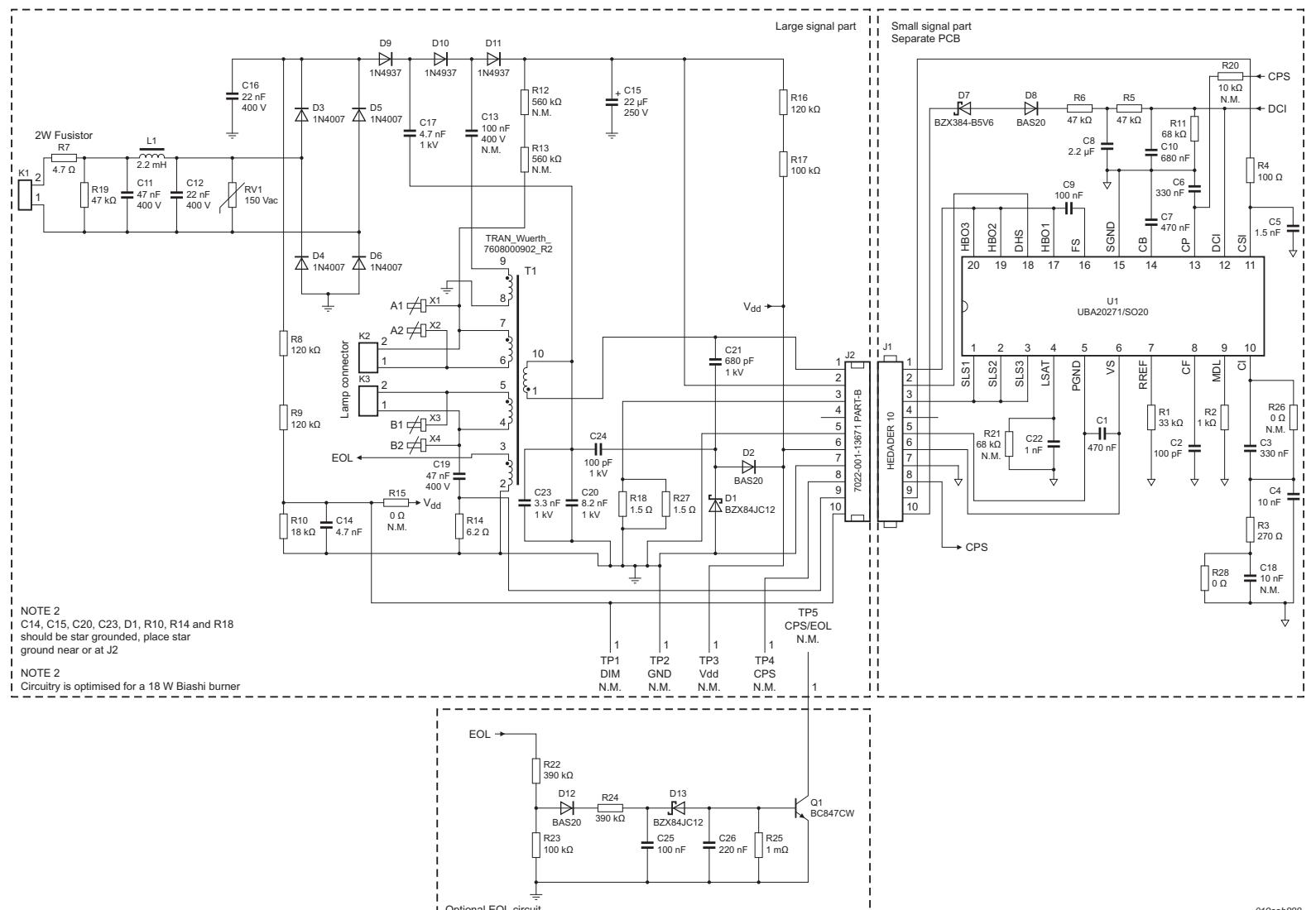
**Fig 23. 20 W 120 V maximum dimmable CFL schematic with UBA20271**

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4.17 18 W maximum 230 V dimmable CFL schematic with UBA20272
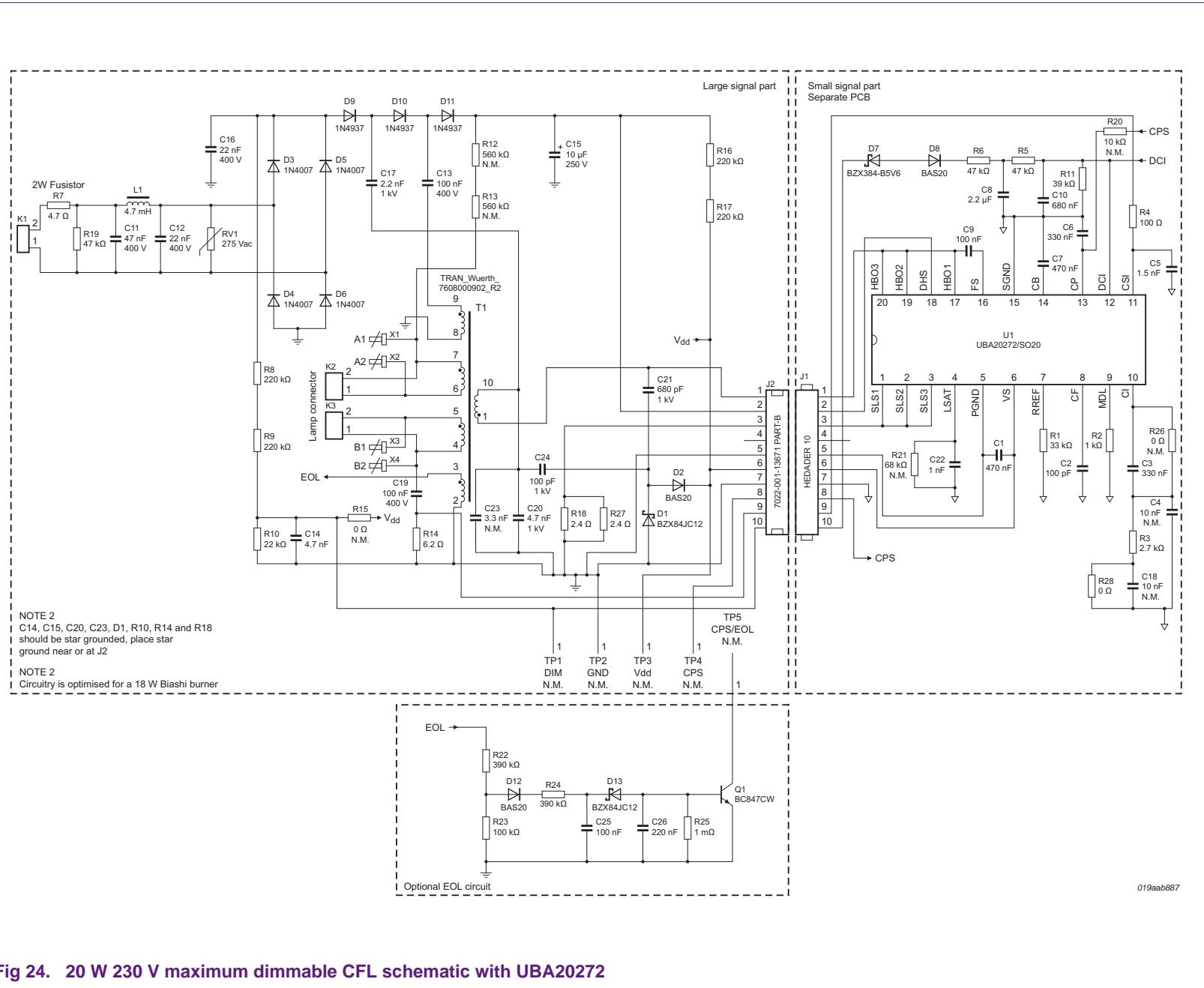
Fig 24. 20 W 230 V maximum dimmable CFL schematic with UBA20272

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5. Appendix 1: Power calculations

$$C_p = 2 \cdot C_{\sec} \cdot \frac{L_{\sec}}{L_{\sec}}$$ (22)

Where: Cp = 2.4×10^{-10} and $\omega_s(f_s) = 2 \cdot \pi \cdot f_s$

$$P_{lamp}(\omega_s) = \frac{V_{lamp}^2}{L_{res} \cdot \omega_s} \cdot \sqrt{\left(\frac{\sqrt{2} \cdot V_{bus}}{\pi \cdot V_{lamp}}\right)^2 \cdot (1 - L_{res} \cdot C_p \cdot \omega_s^2)^2 - [1 - L_{res} \cdot \omega_s^2 \cdot (C_p + C_{res})]^2}$$ (23)

Where: P_{IN} $(2 \cdot \pi \cdot 45000) = 25.144$ and P_{lamp} $(2 \cdot \pi \cdot 45000) = 21.071$

(1) See Equation 24.
(2) See Equation 25.

Fig 25. Lamp power curve

$$P_{lamp}(2 \cdot \pi \cdot f_s)$$ (24)

$$P_{in}(2 \cdot \pi \cdot f_s)$$ (25)

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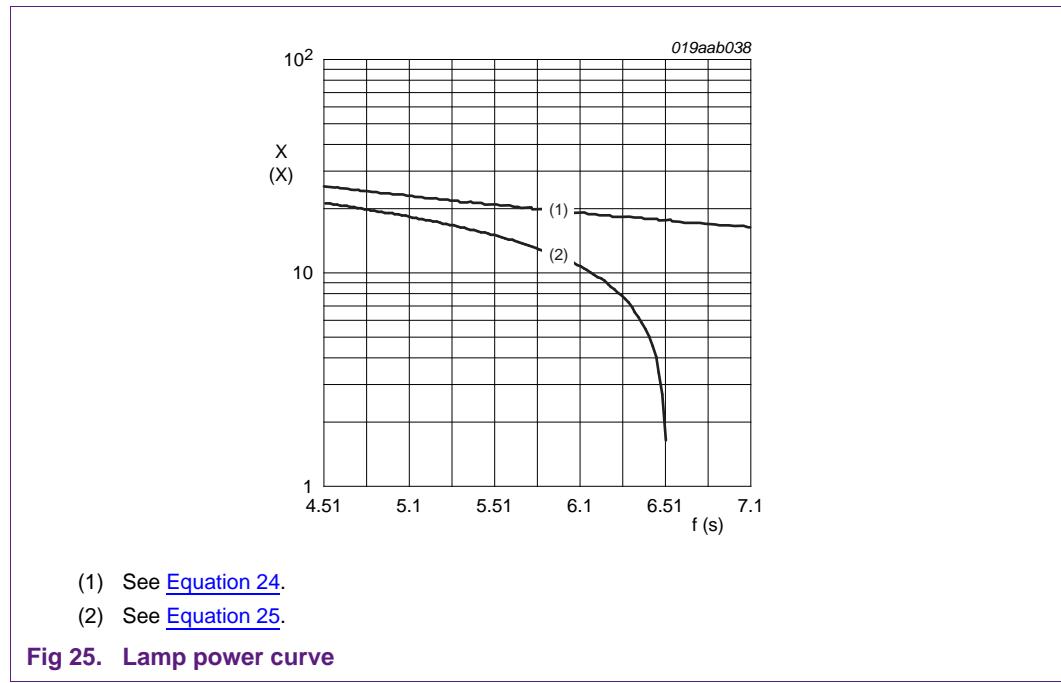
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6.   Appendix 3: Inductive mode preheat calculations

The following values and equations are used for inductive mode preheat calculations. Half-bridge preheat winding are shown in Figure 26 with filament temperature shown in Figure 25.

Where: V_{bus} = 350, t_{hb} = $10 \cdot 10^{-6}$ and t_r = $0.5 \cdot 10^{-6}$

t_r is the time it takes to rise from the minimum to maximum value.

$$f_{hb} = \frac{1}{t_{hb}} \tag{26}$$

Where: f_{hb} = $100 \cdot 10^3$, ω_{hb} = $2 \cdot \pi \cdot f_{hb}$ and ω_{hb} = 628.319×10^3

$$\gamma = \frac{t_r}{t_{hb}} \cdot \pi \tag{27}$$

Where: γ = 0.157, m = 1, 2 to 80 and t = 0, $0.001 \cdot t_{hb}$ to $2 \cdot t_{hb}$

$$V_{hb\_f(m)} = j \frac{V_{bus}}{2 \cdot \pi \cdot \gamma} \cdot \frac{(-1)^m - 1}{m^2} \cdot sin(m\gamma) \tag{28}$$

$$V_{hb\_t}(t) = 2 \cdot Re\left[\sum_{m} (V_{hb\_f}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb} \cdot m \cdot t}) \right] \tag{29}$$

Figure 26 [A] shows that the half-bridge voltage is supplied to the LC filter from which the inductor has two preheat windings. The circuit with the two preheat windings can be redrawn as shown in Figure 26 [B].

a. Inductor with two preheat windings

(1) Related equations see Equation 30, Equation 31 and Equation 31

b. Reduced circuit with two preheat windings

Fig 26. Half-bridge and preheat windings
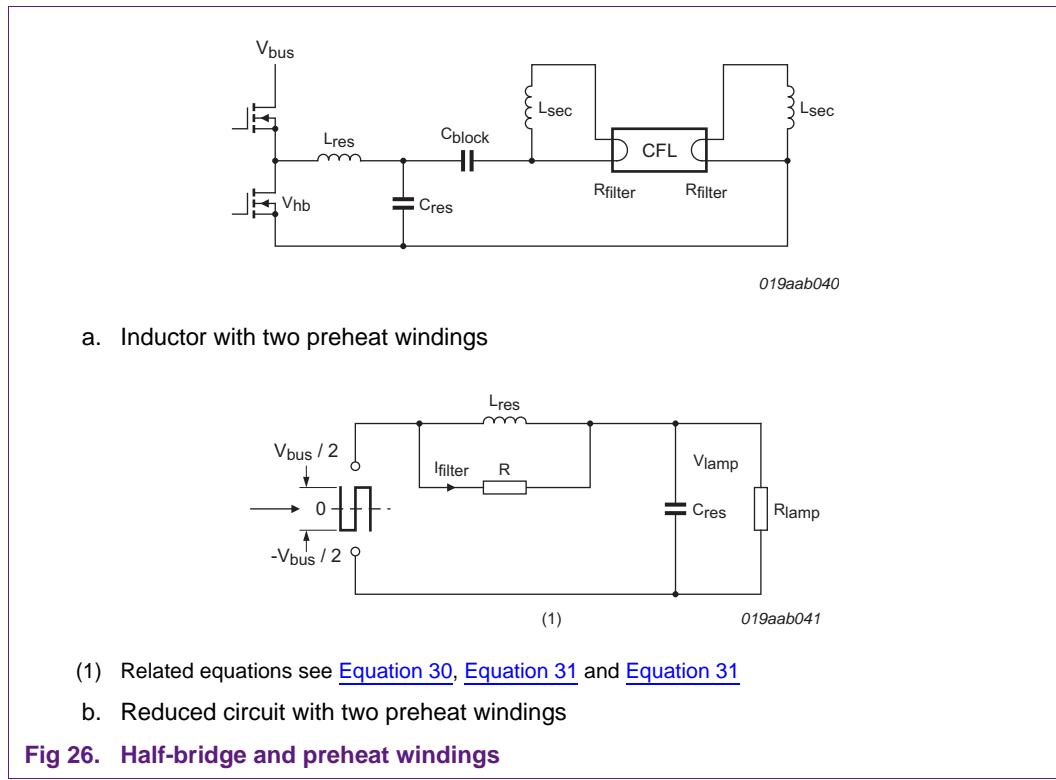
$$R = \frac{1}{2}\frac{L_{res}}{L_{\text{sec}}}R_{filter} \tag{30}$$

$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} \tag{31}$$

Where: L_{res} = 2.75·10^{-3}, L_{sec} = 10·10^{-6}, C_{res} = 4.7·10^{-9} and R_{filter} = 50

$$I_{fil\_f}(m) = \frac{-(m \cdot \omega_{hb})^{2} \cdot L_{res} \cdot C_{res} \cdot \sqrt{\dfrac{L_{\text{sec}}}{L_{res}}}}{j \cdot 2 \cdot m \cdot \omega_{hb} \cdot L_{\text{sec}} + R_{filter} - (m \cdot \omega_{hb})^{2} \cdot L_{res} \cdot C_{res} \cdot R_{filter}} \cdot v_{hb\_f}(m) \tag{32}$$

$$i_{fil(RMS)\text{f}} = \sqrt{2 \cdot \left[\sum_{m}(|i_{fil\_f}(m)|)^{2}\right]} \tag{33}$$

Where: $i_{fil(RMS)\text{f}}$ = 0.18

$$i_{fil\_t} = 2 \cdot Re\left[\sum_{m}(i_{fil\_f}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb} \cdot m \cdot t})\right] \tag{34}$$

7. Abbreviations

Table 5.   Abbreviations

Acronym	Description
CFL	Compact Fluorescent Lamp
CSP	Coil Saturation Protection
CMD	Capacitive Mode Detection
EMI	ElectroMagnetic Interference
OCP	OverCurrent Protection
OVP	OverVoltage Protection
PF	Power Factor
PFC	Power Factor Correction
RLC	Resistance, Inductance, Capacitance
SoS	Sum of Squares
UVLO	UnderVoltage LockOut
VSCP	Voltage Source Charge Pump
ZVS	Zero Voltage Switching

8. References

[1] **AN10803 —** Application note: triac dimmable CFL application using the UBA2028/UBA2014/UBA2027.

[2] **UBA20270 and UBA20271/2 —** Data sheets: dimmable CFL control ICs.

[3] **Power factor correction 1989 IEEE —** Current waveform distortion in power factor correction circuits employing discontinuous mode boost converters.

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